CLAIMS

What is claimed is:

1. A method for determining data stored by a memory cell having a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode coupled to a conductor, comprising the steps of:

floating the bitline;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the bitline is set to a third voltage that is equal to the first voltage minus a threshold voltage of the memory cell; and

sensing the third voltage to determine the data stored by the memory cell.

2. The method of claim 1, further comprising an initial step of setting the bitline to a ground potential.

3. The method of claim 1, wherein the memory cell is a nonvolatile memory cell.

4. A method for simultaneously determining data stored by a plurality of memory cells each having a select gate coupled to a wordline, a first electrode coupled to one of a plurality of bitlines, and a second electrode coupled to a conductor, comprising the steps of:

floating the plurality of bitlines;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the plurality of bitlines is set to a plurality of third voltages, wherein one of the plurality of third voltages is equal to the first voltage minus a threshold voltage of one of the plurality of memory cells; and

sensing the plurality of third voltages to determine the data stored by the plurality of memory cells.

5. The method of claim 4, further comprising an initial step of setting the plurality of bitlines to a ground potential.

6. The method of claim 4, wherein the plurality of memory cells are nonvolatile memory cells.

7. The method of claim 4, wherein determining the data stored by the plurality of memory cells comprises reading a page of data.

8. A method for determining data stored by a memory cell having an adjustable threshold voltage, a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode coupled to a conductor, comprising the steps of:

floating the bitline;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the bitline is set to a third voltage;

determining the adjustable threshold voltage of the memory cell based on the third voltage; and

determining the data stored in the memory cell based on the adjustable threshold voltage of the memory cell.

9. A memory device comprising:

a memory array having data stored in a memory cell, the memory cell having a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode coupled to a conductor; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a first voltage to the wordline and transmitting a second voltage to the conductor such that the bitline is set to a third voltage that is equal to the first voltage minus a threshold voltage of the memory cell, wherein the periphery circuit senses the third voltage to determine the data stored by the memory cell.

10. The memory device of claim 9, wherein the periphery circuit further transmits a ground potential to the bitline before transmitting the first voltage or the second voltage to the memory cell.

11. The memory device of claim 9, wherein the memory cell is a nonvolatile memory cell.

12. The memory device of claim 9, wherein the periphery circuit comprises:

a voltage regulation circuit outputting the first voltage and the second voltage;

a voltage switching circuit coupling the second voltage to the memory cell; and

a sensing circuit coupled to the memory cell, wherein the sensing circuit senses the third voltage to determine the data stored by the memory cell.

13. The memory device of claim 12, further comprising:

a decoder circuit receiving the first voltage from the voltage switching circuit and coupling the first voltage to the memory cell, the decoder circuit decoding a location of the memory cell in the memory array.

14. The memory device of claim 12, further comprising:

a control circuit having read circuitry and write circuitry each coupled to the voltage regulation circuit, the voltage switching circuit, and the ~~sense~~ sensing circuit, wherein the control circuit controls when the first voltage and the second voltage are supplied to the memory cell and when the third voltage is sensed by the ~~sense~~ sensing circuit.

15. The memory device of claim 12, wherein the sensing circuit comprises:

an analog-to-digital converter circuit operative to receive the third voltage and generate a digital value.

16. A memory device comprising:

a memory array having data stored in a plurality of memory cells, the plurality of memory cells each having a select gate coupled to a wordline, a first electrode coupled to one of a plurality of bitlines, and a second electrode coupled to a conductor; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a first voltage to the wordline and transmitting a second voltage to the conductor such that the plurality of bitlines is set to a plurality of third voltages, wherein one of the plurality of third voltages is equal to the first voltage minus a threshold voltage of one of the plurality of memory cells, and wherein the periphery circuit simultaneously senses the plurality of third voltages to determine the data stored by the memory array.

17. A memory device comprising:

a memory array having data stored in a memory cell having an adjustable threshold voltage; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a plurality of voltages to the memory cell and sensing the adjustable threshold voltage of the memory cell to determine the data stored by the memory cell.

18. A memory device comprising:

means having an adjustable threshold voltage for ~~strong~~ data; and

means coupled to the storing means for determining the data stored in the storing means by sensing the adjustable threshold voltage.